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Docket No.
INTL-0296-US

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Transmitted herewith for filing under 35 U.S.C. 111 and 37 C.F.R. 1.53 is the patent application of:

MICHAEL J. McTAGUE, RAMAN M. SRINIVASAN and BRAD A. BARMORE

For: **ASYMMETRIC DIGITAL SUBSCRIBER LOOP MODEM**

JC564 U.S. PTO 09/471435 12/23/99

Enclosed are:

- ☒ Certificate of Mailing with Express Mail Mailing Label No. **EL515089246US**
- ☒ **Three (3)** sheets of drawings.
- ☐ A certified copy of a application.
- ☒ Declaration ☐ Signed. ☒ Unsigned.
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Multiple Dependent Claims (check if applicable) ☐						$0.00
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Dated: **December 23, 1999**

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(P6509)

APPLICATION

FOR

UNITED STATES LETTERS PATENT

TITLE: ASYMMETRIC DIGITAL SUBSCRIBER LOOP MODEM

INVENTORS: MICHAEL J. McTAGUE, RAMAN M. SRINIVASAN and BRAD A. BARMORE

Express Mail No.: EL515089246US

Date: December 23, 1999

ASYMMETRIC DIGITAL SUBSCRIBER LOOP MODEM

Background

This invention relates generally to systems for asymmetric digital subscriber loop (ADSL) communications.

Modems (short for "modulator demodulator") are used to transfer data between processor-based systems. Generally, modems may be utilized to transmit information between processor-based systems over telephone lines. A pair of modems are coupled through a transport such as a telephone network. Each modem includes a transmitter and a receiver which may be coupled by an elastic store or hybrid. In general, digital information developed by a processor-based system may be converted to analog information for transmission over the transport. Likewise, analog information received from the transport may be converted to digital information for use by the processor-based system. Thus, on each end of the transport, a modem may be provided.

A modem that is used with personal computers, as an example, may be called a remote modem because it is remote from the telephone network's central office. A modem that is provided by a telephone system is generally called a central office modem.

ADSL modems may use frequency division multiplexing (FDM) or echo cancellation (EC) to achieve full duplex operation over a subscriber loop. Discrete multi-tone (DMT) is a multi-carrier modulation technique that may achieve high bandwidth efficiency. A central office ADSL modem transmits a downstream signal to a modem at a remote terminal. The central office modem receives an upstream signal from the remote modem. The upstream and downstream signals use a common transport, typically a telephone line. The upstream signal may carry data on a lower portion of a band of frequencies. The downstream signal may carry data over an upper portion of a band of frequencies. In some embodiments, a wider bandwidth may be utilized for downstream signals than upstream signals.

Existing ADSL modems generally are implemented using two or more integrated circuits. One set of integrated circuits provides most of the digital signal processing and the other provides the analog-to-digital and digital-to-analog conversion. Generally, the two integrated circuits are separated after analog to digital conversion on the receiver side and before the digital-to-analog conversion on the transmitter side.

This means that data is transmitted between the two chips at a relatively high data rate. This high data rate transmission between integrated circuit chips results in more buffering at each chip and more pins are needed to

connect the chips. This increases the cost of each chip. In addition, the high data rate also results in higher system cost due to the impact of higher frequency operation on electromagnetic interference (EMI) shielding and power control.

Thus, there is a continuing need for an ADSL modem that allows data to be more efficiently shared between integrated circuits.

Summary

In accordance with one aspect, an asymmetric digital subscriber loop modem includes a integrated circuit with an analog-to-digital converter that produces data at a relatively higher data rate. A device coupled to said analog-to-digital converter, and contained in said integrated circuit, reduces the higher data rate produced by the analog-to-digital converter to a lower data rate. A multiplexer multiplexes the lower data rate data and control information and transmits the data and control information externally of the integrated circuit.

Other aspects are set forth in the accompanying detailed description and claims.

Brief Description of the Drawings

Figure 1 is a block diagram of one embodiment of the present invention;

Figure 2 is a block showing a digital signal processing (DSP) chip and a codec chip in accordance with one embodiment of the present invention;

Figure 3 shows an example of a clock signal that may be utilized in accordance with one embodiment of the present invention;

Figure 4 shows an example of a synchronization signal which may be utilized to synchronize data multiplexed between the codec and the DSP chips in one embodiment of the present invention;

Figure 5 is a timing diagram showing the data output from the DSP chip to the codec chip in one embodiment of the present invention; and

Figure 6 is a timing diagram showing the data input from the codec chip to the DSP chip in one embodiment of the present invention.

Detailed Description

Referring to Figure 1, a remote modem 10 may be an asymmetric digital subscriber loop (ADSL) modem. The modem 10, in one embodiment of the present invention, may be a so-called g.lite ADSL modem or splitterless modem which does not use a splitter at the remote location. While the present invention illustrates a remote modem, the principles set forth herein can also be utilized at the central office modem. However, because of the high number of remote modems compared to the number of central office

modems, the principles set forth in the present invention are particularly applicable to the design of remote modems which are produced in relatively high volumes.

Thus, referring to Figure 1, the downstream signal 16 from the central office (not shown) is received by the receiver section of the modem 10 and particularly by a coder/decoder (codec) chip 14 and its analog filter 18. In one embodiment of the present invention, the analog filter 18 may be a bandpass filter. The analog filter 18 may be coupled to an analog-to-digital converter 20 that converts the analog signal into a digital signal. The output of the analog-to-digital converter 20 is a relatively higher data rate signal.

A decimation filter 22 produces digital samples at a lower data rate compared to the data rate produced by the analog-to-digital converter 20. A decimation factor of the filter 22 indicates the data rate reduction from the higher data rate produced by the analog-to-digital converter 20. The decimation filter 22 may include a low pass filter and a sample rate compression device, in one embodiment of the invention.

The output signal from the decimation filter 22 may then be transmitted by a multiplexer or serializer 24 externally of the chip 14 to an ensuing digital signal processing (DSP) chip 12. The serializer 24, in one embodiment of the present invention, takes the lower data

rate data produced by the decimation filter 22 and multiplexes it together with control information. The multiplexed control information and data are transmitted to a de-multiplexer or de-serializer 26 on the DSP integrated circuit chip 12 in one embodiment of the invention.

The de-serializer 26 demultiplexes the control information and data and forwards the data to a fast fourier transformer (FFT) 28 and a line decoder 30. The line decoder 30, in one embodiment of the present invention, may be a quadrature amplitude modulator (QAM) decoder. The FFT 28 and line decoder 30 demodulate the input data, separating the digital data by carrier frequency.

A protocol framing and error checking unit 32 completes the reception of the signal. The unit 32 checks for errors and places the data in a particular format for use in connection with a particular processor-based system (not shown). The decoded data stream is then passed to an elastic store or hybrid 34. A link 36 provides the information to a processor-based system (not shown).

Transmit data 54 (from the processor-based system) heading upstream goes through a transmitter section including a protocol framing and error coding unit 38 into a line encoding unit 40. The line encoding unit 40 may be a quadrature amplitude modulator (QAM) encoder, in one embodiment of the present invention. After line encoding,

the information is processed by an inverse fast Fourier transformer (IFFT). The data is selectively encoded by the encoder 40 at a relatively higher data rate and the IFFT produces, for each frame, a sequence of digital samples at a relatively lower data rate.

The lower data rate output signal from the IFFT 42 is provided to a multiplexer or serializer 44 which transmits the data together with control information over a link 45 to a de-serializer 46 on the chip 14. The serializer 44 may provide a multiplexing function. The output of the de-serializer 46 is interpolated by an interpolation filter 48. The filter 48 adds interpolated data into the data stream distributed by the modem to reduce the effect of imaging by increasing the rate at which samples are produced.

Thus, the interpolation filter 48 increases the data rate of the data intended for the upstream signal 54. The interpolation filter 48 may include digital low pass filtering that enables digital suppression of the lower frequency images in the interpolation filter 48 so that the remaining images may be more easily and effectively removed by the analog filter 52. In one embodiment of the present invention, the analog filter 52 may be a low pass filter. A digital-to-analog converter 50 converts the digital signal from the interpolation filter 48 into a analog signal that is filtered by the analog filter 52.

The chips 12 and 14 communicate at lower data rates. This use of lower data rate communication may have the effect, in some embodiments of the present invention, of reducing the buffering required in each chip 12 and 14. This may reduce the cost of the overall modem 10. In addition, by reducing the data rate on the links 45 and 25, system cost may be reduced due to the impact of lower frequency operation and diminished need for EMI shielding and power control. Since the reduced data rates were used for other reasons in both the receiver and transmitter sections, no substantial additional costs are incurred.

In some embodiments of the present invention, the operation of the chip 12 may be accomplished in software implementing a soft modem. In such case, the DSP chip 12 may be eliminated. In a soft modem, a chip may be used to provide an interface between a system bus in the processor-based system and the codec chip 14.

Referring next to Figure 2, in accordance with one embodiment of the present invention, a coder/decoder (codec) chip 14 may include a clock control interface 60 and a link controller 25a, 45a to the link 25. The link 25 may communicate with a link controller 25a on a DSP chip 12. A DSL clock 72 may be controlled by control 74 coupled to a control (out-of-band) data stream 76. A sample (in-band) data stream 78 may couple the link controller 25a, 45a to the codec functions 80. The DSL clock 72 may be

implemented in the codec chip 14, DSP chip 12 or as a stand alone device, as shown in Fig. 2. With a stand alone device, the control signals for the clock function may come from software. However, a digital analog (D/A) converter is used for clock control. If the D/A converter is in the codec chip 14, the link may be used to carry the clock D/A sample data.

The DSP chip 12 may include a system interface 58 that interfaces with a system bus 56 in a processor-based system (not shown). A sample (in-band) data stream 82 may flow between the interface 58 and DSP functions 84 and on to the controller 25a, 45a. A control (out-of-band) data stream 86 may flow between the interface 58 and the controller 25a, 45a.

The signals on the links 25 and 45 include the data paths 62 and 64 which provide receive (data in) and transmit (data out) data at reduced data rates as described previously. In addition, control information in the form of a synchronization signal 66, clock information 68 and reset information 70 may also be provided in the multiplexed stream.

Thus, the links 25, 45 may provide a serial interface which carries the data in and data out signals 62 and 64, a clock signal 68, a synchronization signal 70 and a reset signal 70. Examples of hypothetical data in and data out signals are shown in Figures 5 and 6, respectively. A

hypothetical synchronization signal is illustrated in Figure 4, and a hypothetical clock signal as illustrated in Figure 3.

In the case of a soft modem embodiment, the DSP 12, shown in Figure 2, may be eliminated. However, the links 25a, 25b, 45a, 45b and the interface 58 may still be used in some embodiments.

Thus, full duplex data flow may be achieved. The data frame may include a header that indicates the validity of the entire frame and also the validity of each cell within the frame. A header may also be needed to distinguish sample data from control data on the link. One instantiation of the frame uses a two bit header and a fourteen bit payload, as shown in Figures 5 and 6. A common clock and synchronization pulse may be utilized for both data intended for downstream and upstream communications. In one embodiment of the present invention, the system may implement a so-called g.lite ADSL modem. However, other ADSL modems may be implemented as well including splitterless modems and modems including splitters.

While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended

claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is:

1. An asymmetric digital subscriber loop modem comprising:

an integrated circuit;

an analog-to-digital converter contained in said integrated circuit, said converter producing data at a relatively higher data rate;

a device contained in said circuit and coupled to said analog-to-digital converter, said device reducing the higher data rate data from the analog-to-digital converter to a lower data rate; and

a multiplexer that multiplexes said lower data rate data and control information and transmits said data and control information externally of said integrated circuit.

2. The modem of claim 1 including a second integrated circuit, said second integrated circuit including a de-multiplexer that de-multiplexes said lower data rate data and said control information.

3. The modem of claim 1 wherein said device includes a decimation filter.

4. The method of claim 3 wherein said integrated circuit includes a analog filter coupled to said analog-to-

digital converter in turn coupled to said decimation filter in turn coupled to said multiplexer.

5. The modem of claim 1 wherein said integrated circuit further includes a demultiplexer coupled to a device that increases the data rate of data received by said demultiplexer, said device that increases the data rate being coupled to a digital-to-analog converter.

6. The modem of claim 5 wherein said device for increasing the data rate includes an interpolation filter.

7. The modem of claim 1 wherein said integrated circuit includes both a receiver section and a transmitter section.

8. The modem of claim 1 including a second integrated circuit having a receiver section coupled to receive said lower data rate data and control information from said integrated circuit.

9. The modem of claim 8 wherein said second integrated circuit implements discrete multi-tone modulation.

10. The modem of claim 9 wherein said second integrated circuit provides digital signal processing.

11. The modem of claim 9 wherein said second integrated circuit includes a fast Fourier transformer and a line decoder.

12. The modem of claim 1 including a second integrated circuit, said second integrated circuit including a line encoder which produces data at a relatively higher data rate and a device coupled to said line encoder that produces data at a relatively lower data rate, said device being coupled to a serializer which transmits said data to said integrated circuit.

13. The modem of claim 12 wherein said device is an inverse fast Fourier transformer.

14. A method comprising:

receiving analog data on a first integrated circuit device;

converting said analog data to digital format;

decreasing the data rate of said data;

serializing said data; and

transmitting said data to a second integrated circuit device.

15. The method of claim 14 wherein reducing the data rate of said digital data includes decimating said digital data.

16. The method of claim 15 wherein serializing said data includes multiplexing said data with control information.

17. The method of claim 16 further including receiving said data on said second integrated circuit and de-serializing said data.

18. The method of claim 17 including increasing the data rate of said data on said second integrated circuit.

19. The method of claim 18 wherein increasing said data rate includes fast fourier transforming said data.

20. The method of claim 14 further including receiving digital data for transmission by said first chip and increasing the data rate of said data.

21. The method of claim 20 wherein increasing said data rate includes interpolating said data.

22. The method of claim 21 including converting said interpolated data to an analog format signal.

23. An asymmetric digital subscriber loop modem comprising:

a first integrated circuit including an analog-to-digital converter, a device to reduce the data rate from the analog-to-digital converter to a lower data rate, and a serializer; and

a second integrated circuit, said serializer transmitting said lower data rate data from said first integrated circuit to said second integrated circuit, said second integrated circuit including a de-serializer that receives said lower data rate data from said first integrated circuit and transmits said data to a device for demodulating said data.

24. The modem of claim 23 wherein said second integrated circuit includes a modulating circuit which decreases the data rate of digital data and a serializer which transmits said decreased data rate data to said first integrated circuit, said first integrated circuit including a de-serializer that receives said modulated data, said de-serializer coupled to a device that increases the data rate of said data, said device coupled to a digital-to-analog converter.

25. The modem of claim 23 wherein said device on said first integrated circuit for decreasing the data rate of said data is a decimation filter.

26. The modem of claim 24 wherein said device that increases the data rate on said first integrated circuit is an interpolation filter.

27. The modem of claim 24 wherein said modulating circuit includes an inverse fast Fourier transformer.

28. The modem of claim 23 wherein said modem is a splitterless remote modem.

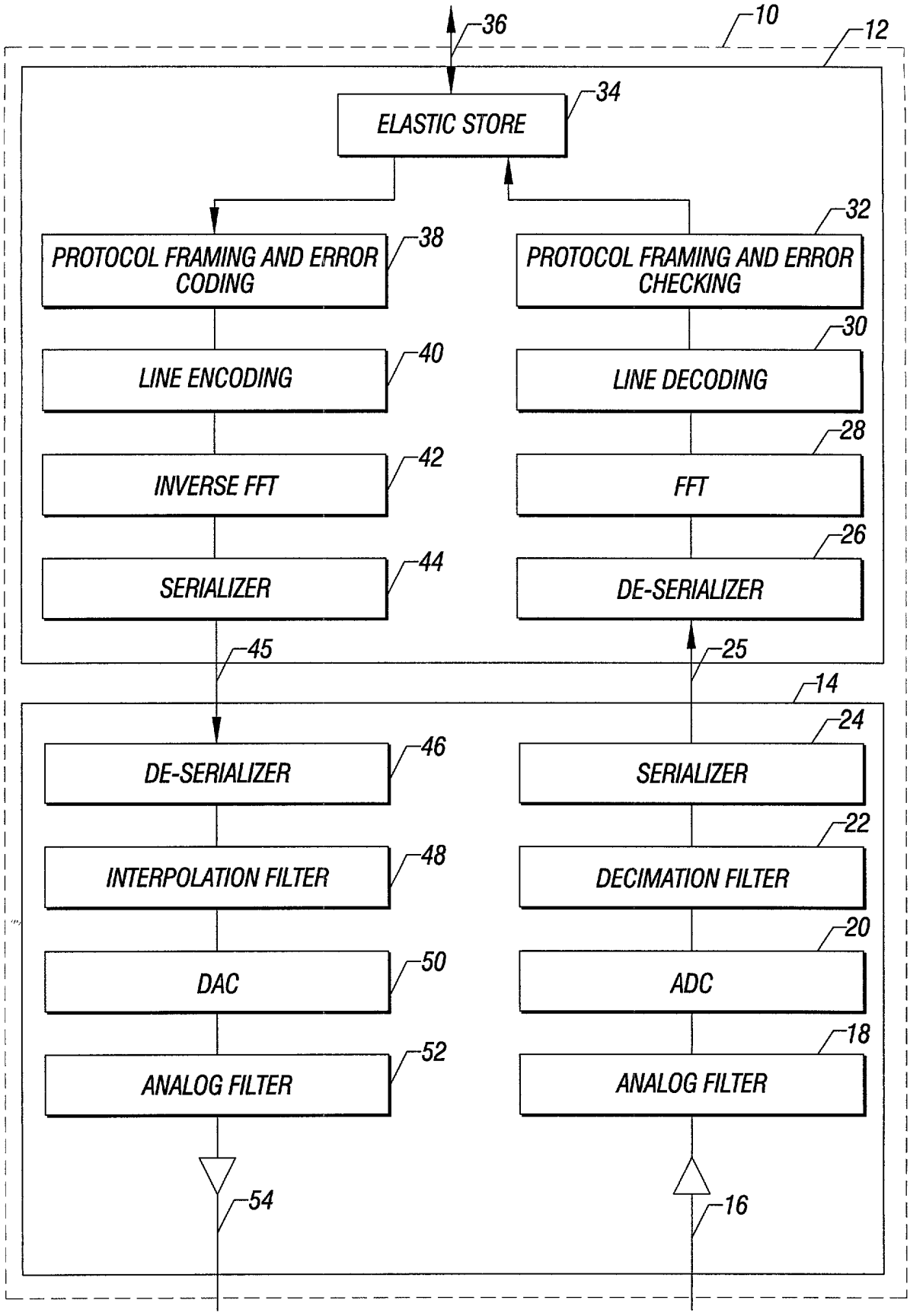
29. The modem of claim 23 wherein said serializer multiplexes lower data rate data and control information.

30. The modem of claim 23 wherein lower data rate data is transmitted in two directions between said first and second integrated circuits.

ASYMMETRIC DIGITAL SUBSCRIBER LOOP MODEM

Abstract of the Disclosure

An asymmetric digital subscriber loop modem may achieve efficiency and cost reduction by providing a coder/decoder (codec) chip which transmits data externally of the chip when the data is at a reduced or lower data rate. That is, instead of transmitting the data at a higher data rate, which may result in increased cost, for example for EMI shielding, the codec chip transmits the data when the data is at a reduced data rate.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PROTOCOL FRAMING AND ERROR CHECKING
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LINE DECODING
30
INVERSE FFT
42
FFT
28
SERIALIZER
44
DE-SERIALIZER
26
45
25
14
DE-SERIALIZER
46
SERIALIZER
24
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ANALOG FILTER
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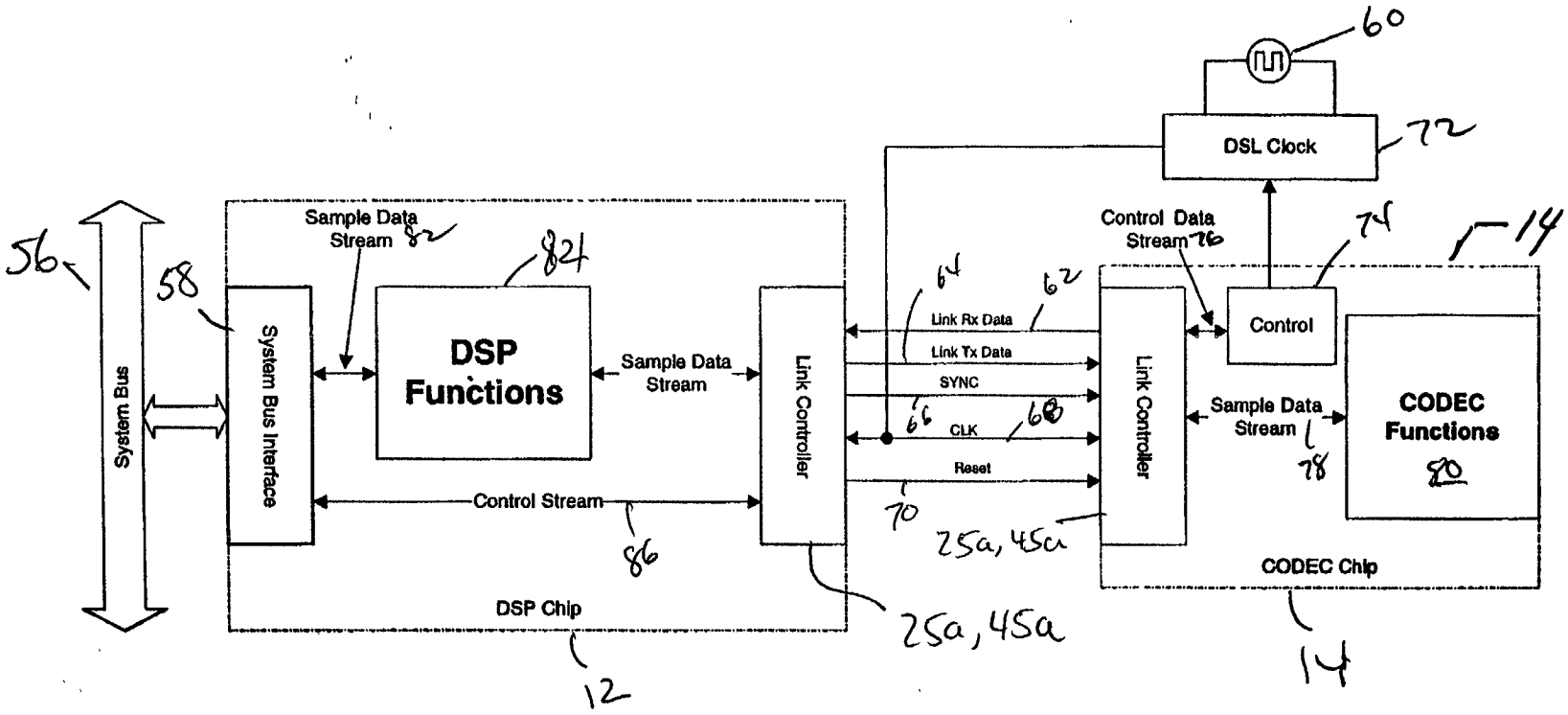
ANALOG FILTER
18
54
16

FIG. 1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74
14
56
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System Bus
System Bus Interface
Sample Data Stream
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DSP Functions
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64
62
Link Rx Data
Link Tx Data
SYNC
CLK
66
68
Reset
70
Control Stream
86
DSP Chip
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Link Controller
Control
Sample Data Stream
78
CODEC Functions
80
CODEC Chip
14

Fig 2

Fig 3

Fig 4

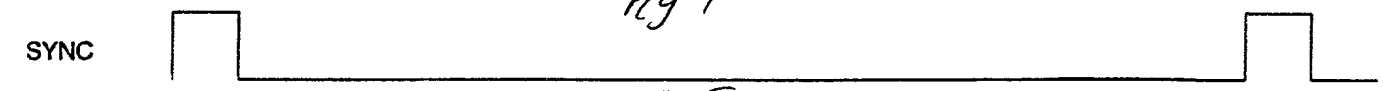

Fig 5

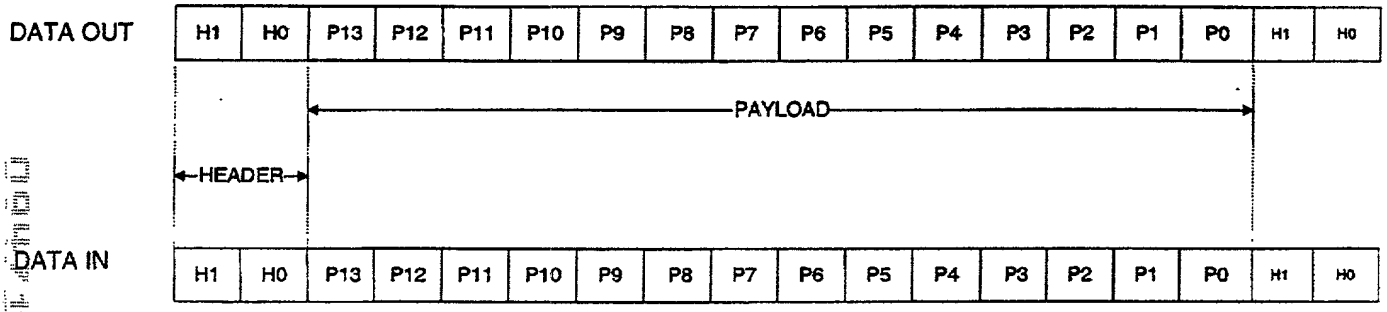

Fig 6

Attorney's Docket No.: INTL-0296 -US (P6509) PATENT

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

ASYMMETRIC DIGITAL SUBSCRIBER LOOP MODEM

the specification of which

X	is attached hereto.
	was filed on _____ as United States Application Number _____ or PCT International Application Number _____ and was amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):			Priority Claimed	
Number	(Country)	(Day/Month/Year Filed)	Yes	No
Number	(Country)	(Day/Month/Year Filed)	Yes	No
Number	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under title 35, United States Code, Section 119(e) of the United States provisional application(s) listed below:

(Application Number)	(Filing Date)
(Application Number)	(Filing Date)

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

(Application Number)	Filing Date	(Status-patented, pending, abandoned)
(Application Number)	Filing Date	(Status-patented, pending, abandoned)

I hereby appoint Timothy N. Trop, Reg. No. 28,994; Fred G. Pruner, Jr., Reg. No. 40,779, Dan C. Hu, Reg. No. 40,025; Coe F. Miles, Reg. No. 38,559, and John R. Merkling, Reg. No. 31,716 my patent attorneys, of TROP, PRUNER, HU & MILES, P.C., with offices located at 8554 Katy Freeway, Ste. 100, Houston, TX 77024, telephone (713) 468-8880, and Joseph R. Bond, Reg. No. 36,458; Richard C. Calderwood, Reg. No. 35,468; Sean Fitzgerald, Reg. No. 32,027; David J. Kaplan, Reg. No. 41,105; Leo V. Novakoski, Reg. No. 37,198; Naomi Obinata, Reg. No. 39,320; Thomas C. Reynolds, Reg. No. 32,488; Steven P. Skabrat, Reg. No. 36,279; Howard A. Skaist, Reg. No. 36,008; Steven C. Stewart, Reg. No. 33,555; Raymond J. Werner, Reg. No. 34,752; and Charles K. Young, Reg. No. 39,425; my patent attorneys, of INTEL CORPORATION; with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to Timothy N. Trop, TROP, PRUNER, HU & MILES, P.C., 8554 Katy Freeway, Ste. 100, Houston, TX 77024 and direct telephone calls to Timothy N. Trop, (713) 468-8880.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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